ABSTRACT OF THE DISCLOSURE

A chip-join process to reduce elongation mismatch between the adherents involves thermally expanding each of a coefficient of thermal expansion mismatched semiconductor chip and substrate a substantially equal amount from their room temperature state in a direction along surfaces thereof to be joined by soldering. The thermally expanded semiconductor chip and substrate are then soldered to one another forming a plurality of soldered joints, and then cooled to room temperature. The process enables elongation mismatch from soldering to be reduced to less than half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature following soldering, thereby reducing post soldering residual stress, residual plastic deformation in the soldered joints, residual plastic deformation in the substrate, and semiconductor chip warpage.